

Pin Designations for Popular Buses

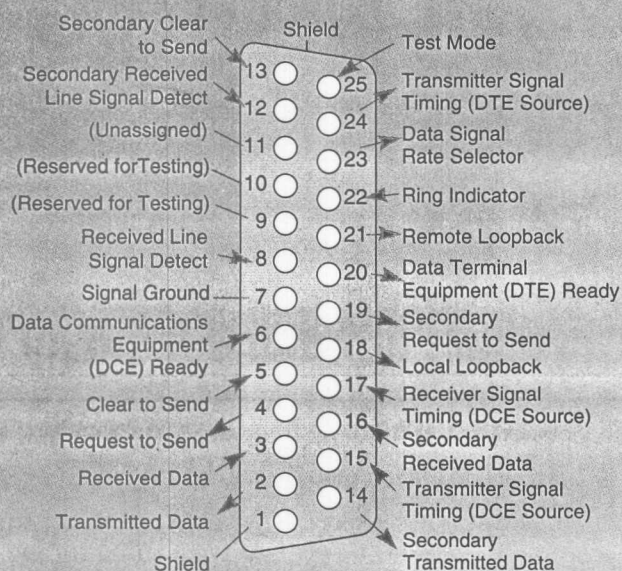
Computer communications—whether between a host and its plug-in cards, between two computers, or between a computer and instruments—require some form of bus signals and protocols. The most commonly used computer buses in test and measurement are the RS-232C serial bus, the IEEE 488 bus, the VXIbus, and

the ISA bus used in personal computers. An emerging computer bus is the PCI bus, a high-speed bus for host computers to communicate with plug-in cards.

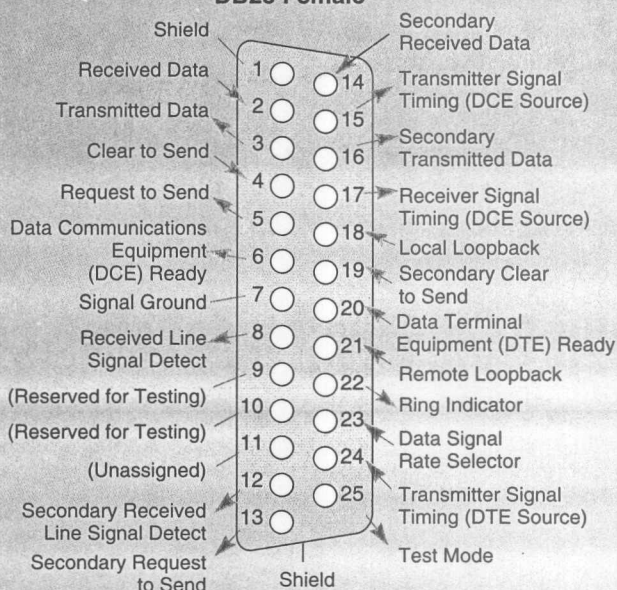
The following pages give you the signal-pin configurations for these popular buses. You'll also find a table of ASCII characters—one of those references you always seem to need.

RS-232C* Pin Designations

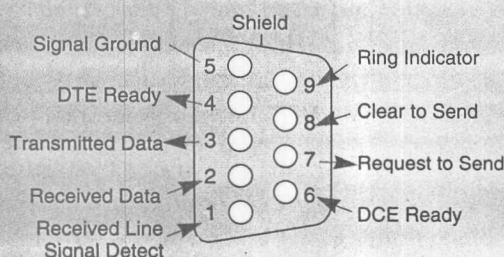
DB25 Male



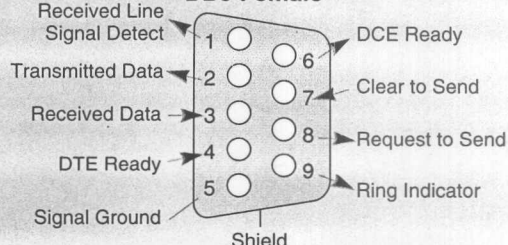
DB25 Female



DB9 Male



DB9 Female



* Also known as EIA-232

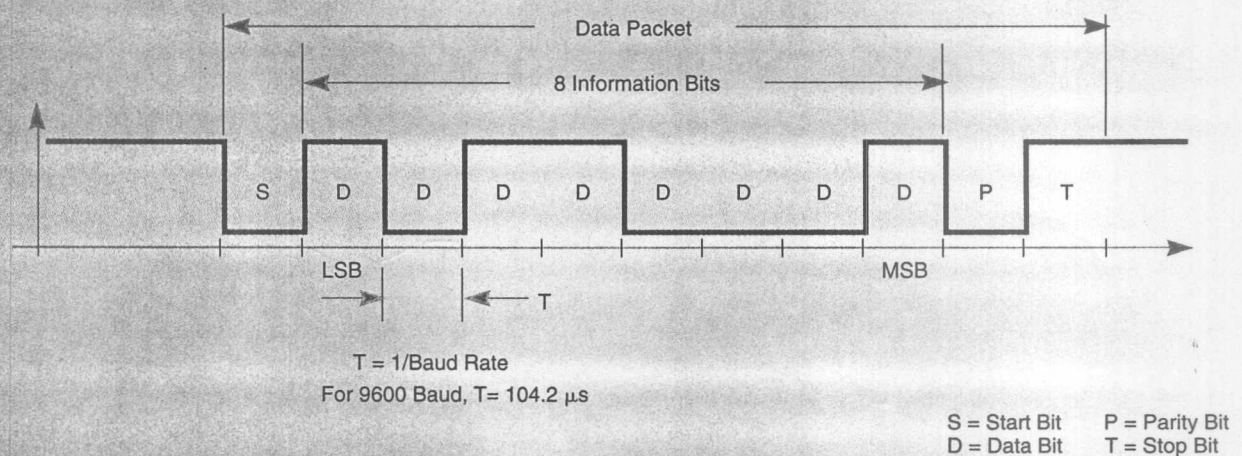
ASCII Character Set

Hex	Dec	Character	Hex	Dec	Character	Hex	Dec	Character	Hex	Dec	Character
00	00	NUL	20	32	space	40	64	@	60	96	`
01	01	SOH	21	33	!	41	65	A	61	97	a
02	02	STX	22	34	"	42	66	B	62	98	b
03	03	ETX	23	35	#	43	67	C	63	99	c
04	04	EOT	24	36	\$	44	68	D	64	100	d
05	05	ENQ	25	37	%	45	69	E	65	101	e
06	06	ACK	26	38	&	46	70	F	66	102	f
07	07	BEL	27	39	'	47	71	G	67	103	g
08	08	BS	28	40	(48	72	H	68	104	h
09	09	HT	29	41)	49	73	I	69	105	i
0A	10	LF	2A	42	*	4A	74	J	6A	106	j
0B	11	VT	2B	43	+	4B	75	K	6B	107	k
0C	12	FF	2C	44	,	4C	76	L	6C	108	l
0D	13	CR	2D	45	-	4D	77	M	6D	109	m
0E	14	SO	2E	46	.	4E	78	N	6E	110	n
0F	15	SI	2F	47	/	4F	79	O	6F	111	o
10	16	DLE	30	48	0	50	80	P	70	112	p
11	17	DC1	31	49	1	51	81	Q	71	113	q
12	18	DC2	32	50	2	52	82	R	72	114	r
13	19	DC3	33	51	3	53	83	S	73	115	s
14	20	DC4	34	52	4	54	84	T	74	116	t
15	21	NAK	35	53	5	55	85	U	75	117	u
16	22	SYN	36	54	6	56	86	V	76	118	v
17	23	ETB	37	55	7	57	87	W	77	119	w
18	24	CAN	38	56	8	58	88	X	78	120	x
19	25	EM	39	57	9	59	89	Y	79	121	y
1A	26	SUB	3A	58	:	5A	90	Z	7A	122	z
1B	27	ESC	3B	59	;	5B	91	[7B	123	{
1C	28	FS	3C	60	<	5C	92	\	7C	124	
1D	29	GS	3D	61	=	5D	93]	7D	125	}
1E	30	RS	3E	62	>	5E	94	^	7E	126	~
1F	31	US	3F	63	?	5F	95	_	7F	127	DEL

ASCII Control Codes

NUL	Null	VT	Vertical Tab	SYN	Synchronous Idle
SOH	Start of Heading	FF	Form Feed	ETB	End of Transmission Block
STX	Start of Text	CR	Carriage Return	CAN	Cancel
ETX	End of Text	SO	Shift Out	EM	End of Medium
EOT	End of Transmission	SI	Shift In	SUB	Substitute
ENQ	Enquiry	DLE	Data Link Escape	ESC	Escape
ACK	Acknowledge	DC1	Device Control 1	FS	File Separator
BEL	Bell	DC2	Device Control 2	GS	Group Separator
BS	Back Space	DC3	Device Control 3	RS	Record Separator
HT	Horizontal Tab	DC4	Device Control 4	US	Unit Separator
LF	Line Feed	NAK	Negative Acknowledge	DEL	Delete

Serial Asynchronous Timing Diagram



VXIbus Pin Designations

Signal Definitions

Axx Address bit
ACFAIL AC Power Failure
AMx Address Modifier
BBSY Bus Busy
BCLR Bus Clear
BERR Bus Error
BGx Bus Grant
BRx Bus Request
CLK10 Clock 10

Dxx Data Bit
DTACK Data Transfer Acknowledge
ECLTRGx ECL Trigger
IACK* Interrupt Acknowledge
IRQx* Interrupt Request
LBUSxxx Local Bus Bit
LWORD Long Word
MODIDxx Module ID Bit

RSVx Reserved
SERCLK Unused
SERDAT Unused
SUMBUS Analog Summing Node
SYSCLK System Clock
SYSFAIL System Failure
SYSRESET System Reset
TTLTRGx* TTL Trigger

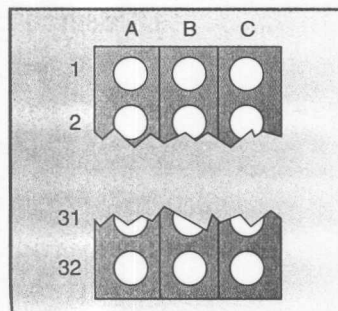
VXIbus P1 Pin Designations

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK	A17
22	IACKOUT*	SERDAT*	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12 V	+5 V STDBY	+12 V
32	+5 V	+5 V	+5 V

VXIbus P2 Pin Designations

Pin Number	Slot 0 Row A Signal Mnemonic	Slots 1-12 Row A Signal Mnemonic	Slots 0-12 Row B Signal Mnemonic	Row C Signal Mnemonic
1	ECLTRG0	ECLTRG0	+5 V	CLK10+
2	-2 V	-2 V	GND	CLK10-
3	ECLTRG1	ECLTRG1	RSV1	GND
4	GND	GND	A24	-5.2 V
5	MODID12	LBUSA00	A25	LBUSC00
6	MODID11	LBUSA01	A26	LBUSC01
7	-5.2 V	-5.2 V	A27	GND
8	MODID10	LBUSA02	A28	LBUSC02
9	MODID09	LBUSA03	A29	LBUSC03
10	GND	GND	A30	GND
11	MODID08	LBUSA04	A31	LBUSC04
12	MODID07	LBUSA05	GND	LBUSC05
13	-5.2 V	-5.2 V	+5 V	-2 V
14	MODID06	LBUSA06	D16	LBUSC06
15	MODID05	LBUSA07	D17	LBUSC07
16	GND	GND	B18	GND
17	MODID04	LBUSA08	D19	LBUSC08
18	MODID03	LBUSA09	D20	LBUSC09
19	-5.2 V	-5.2 V	D21	-5.2 V
20	MODID02	LBUSA10	D22	LBUSC10
21	MODID01	LBUSA11	D23	LBUSC11
22	GND	GND	GND	GND
23	TTLTRG0*	TTLTRG0*	D24	TTLTRG1*
24	TTLTRG2*	TTLTRG2*	D25	TTLTRG3*
25	+5 V	+5 V	D26	GND
26	TTLTRG4*	TTLTRG4*	D27	TTLTRG5*
27	TTLTRG6*	TTLTRG6*	D28	TTLTRG7*
28	GND	GND	D29	GND
29	RSV2	RSV2	D30	RSV3
30	MODID00	MODID	D31	GND
31	GND	GND	GND	+24 V
32	SUMBUS	SUMBUS	+5 V	-24 V

Courtesy of Kinetic Systems

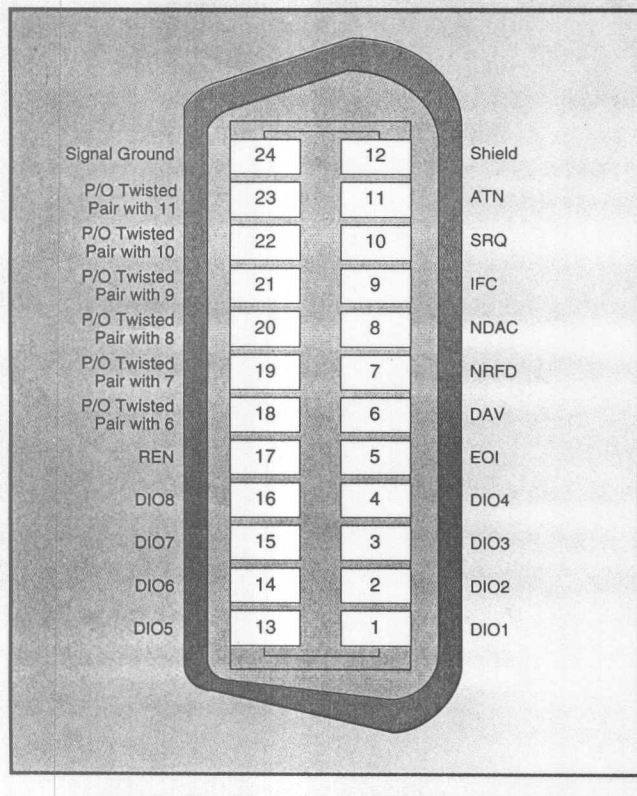


Physical alignment for P1 and P2
As seen from front of back plane

IEEE 488 Bus Pin Designations

Signal Definitions

ATN	Attention
DAV	Data Valid
DIOx	Data I/O bits
EOI	End or Identify
IFC	Interface Clear
NDAC	Not Data Accepted
NRFD	Not Ready for Data
REN	Remote Enable
SRQ	Service Request



For More Information

To get more information about these and other pin designations, contact the following organizations:

EIA (Electronics Industries Association), Arlington, VA. 703-907-7500.

IEEE (Institute of Electrical and Electronics Engineers), New York, NY. 212-705-7900.

ISA (The International Society for Measurement and Control), Research Triangle Park, NC. 919-549-8411.

PC/104 Consortium, Mt. View, CA. 415-903-8304.

PCI Special Interest Group, Portland, OR. 800-433-5177.

STDBus Manufacturers' Group, Apex, NC. 919-387-7351.

VME International Trade Association, Scottsdale, AZ. 602-951-8866.

VXibus Consortium, La Mesa, CA. 619-697-6650.

ISA Bus Pin Designations

Signal Definitions

AEN	Access Cycle Enable
BALE	Bus Address Latch Enable
DACKx	Data Acknowledge
DRQx	DMA Request
ENDXFR*	End transfer
IOCHCHK*	Error on bus
IOCHRDY	I/O Channel Ready
IOCS16*	Accessed 16-bit I/O resource
IOR*	I/O read
IOW*	I/O Write
IRQxx	Interrupt Request
LAXx	16 Megabyte Memory
MEMCS16*	Accessed 16-bit Memory resource
OSC	Oscillator
REFRESH*	Refresh Cycle
SAxx	Address
SBHE*	Valid Data on SD-15>
SDxx	Data
SMEMR*	First Megabyte Memory Read
SMEMW*	First Megabyte Memory Write
SYSCLK	System Clock

Signal	Pin	Pin	Signal
0 V	B01	A01	IOCHCHK*
RESETDRV	B02	A02	SD7
+5	B03	A03	SD6
IRQ9 (KEY)	B04	A04	SD5
-5	B05	A05	SD4
DRQ2	B06	A06	SD3
-12 V	B07	A07	SD2
ENDXFR*	B08	A08	SD1
+12 V	B09	A09	SD0
0 V	B10	A10	IOCHRDY
SMEMW*	B11	A11	AEN
SMEMR*	B12	A12	SA19
IOW*	B13	A13	SA18
IOR*	B14	A14	SA17
DACK3*	B15	A15	SA16
DRQ3	B16	A16	SA15
DACK1*	B17	A17	SA14
DRQ1*	B18	A18	SA13
REFRESH*	B19	A19	SA12
SYSCLK	B20	A20	SA11
IRQ7	B21	A21	SA10
IRQ6	B22	A22	SA9
IRQ5	B23	A23	SA8
IRQ4	B24	A24	SA7
IRQ3	B25	A25	SA6
DACK2*	B26	A26	SA5
TC	B27	A27	SA4
BALE	B28	A28	SA3
+5 V	B29	A29	SA2
OSC	B30	A30	SA1
0 V	B31	A31	SA0
MEMCS16*	D01	C01	SBHE*
IOCS16*	D02	C02	LA23
IRQ10	D03	C03	LA22
IRQ11	D04	C04	LA21
IRQ12	D05	C05	LA20
IRQ15	D06	C06	LA19
IRQ14	D07	C07	LA18
DACK0*	D08	C08	LA17
DRQ0	D09	C09	MEMR*
DACK5*	D10	C10	MEMW*
DRQ5	D11	C11	SD8
DACK6*	D12	C12	SD9
DRQ6	D13	C13	SD10
DACK7*	D14	C14	SD11
DRQ7	D15	C15	SD12
+5 V	D16	C16	SD13
MASTER*	D17	C17	SD14
0 V	D18	C18	SD15

Bracket End

Add-in Board Component Side

-12 V	B01	A01	TRST*
TCK	B02	A02	+12 V
GND	B03	A03	TMS
TDO	B04	A04	TDI
+5 V	B05	A05	+5 V
+5 V	B06	A06	INTA*
INTB*	B07	A07	INTC*
INTD*	B08	A08	+5 V
REQ3*	B09	A09	CLKC
REQ1*	B10	A10	Note 1
GNT3*	B11	A11	CLKD
Note 2	B12	A12	Note 2
Note 2	B13	A13	Note 2
CLKA	B14	A14	GNT1*
GND	B15	A15	RST*
CLKB	B16	A16	Note 1
GND	B17	A17	GNT0*
REQ0*	B18	A18	GND
Note 1	B19	A19	REQ2*
AD31	B20	A20	AD30
AD29	B21	A21	+3.3 V
GND	B22	A22	AD28
AD27	B23	A23	AD26
AD25	B24	A24	GND
+3.3 V	B25	A25	AD24
C/BE3*	B26	A26	GNT2*
AD23	B27	A27	+3.3 V
GND	B28	A28	AD22
AD21	B29	A29	AD20
AD19	B30	A30	GND
+3.3 V	B31	A31	AD18
AD17	B32	A32	AD16
C/BE2*	B33	A33	+3.3 V
GND	B34	A34	FRAME*
IRDY*	B35	A35	GND
+3.3 V	B36	A36	TRDY*
DEVSEL*	B37	A37	GND
GND	B38	A38	STOP*
LOCK*	B39	A39	+3.3 V
PERR*	B40	A40	SDONE
+3.3 V	B41	A41	SBO*
SERR*	B42	A42	GND
+3.3 V	B43	A43	PAR
C/BE1*	B44	A44	AD15
AD14	B45	A45	+3.3 V
GND	B46	A46	AD13
AD12	B47	A47	AD11
AD10	B48	A48	GND
Note 3	B49	A49	AD09
Note 4	B50	A50	Note 4
Note 4	B51	A51	Note 4
AD08	B52	A52	C/BE0*
AD07	B53	A53	+3.3 V
+3.3 V	B54	A54	AD06
AD05	B55	A55	AD04
AD03	B56	A56	GND
GND	B57	A57	AD02
AD01	B58	A58	AD00
Note 1	B59	A59	
ACK64*	B60	A60	REQ64*
+5 V	B61	A61	+5 V
+5 V	B62	A62	+5 V

PCI 32-bit connector end

PCI 64-bit connector start

Reserved	B63	A63	GND
GND	B64	A64	C/BE7*
C/BE6*	B65	A65	C/BE5*
C/BE4*	B66	A66	Note 1
GND	B67	A67	PAR64
AD63	B68	A68	AD62
AD61	B69	A69	GND
Note 1	B70	A70	AD60
AD59	B71	A71	AD58
AD57	B72	A72	GND
GND	B73	A73	AD56
AD55	B74	A74	AD54
AD53	B75	A75	Note 1
GND	B76	A76	AD52
AD51	B77	A77	AD50
AD49	B78	A78	GND
Note 1	B79	A79	AD48
AD47	B80	A80	AD46
AD45	B81	A81	GND
GND	B82	A82	AD44
AD43	B83	A83	AD42
AD41	B84	A84	Note 1
GND	B85	A85	AD40
AD39	B86	A86	AD38
AD37	B87	A87	GND
Note 1	B88	A88	AD36
AD35	B89	A89	AD34
AD33	B90	A90	GND
GND	B91	A91	AD32
Reserved	B92	A92	Reserved
Reserved	B93	A93	GND
GND	B94	A94	Reserved

Notes

1. On +5-V-only boards, these pins are designated +5 V; on 3.3-V boards, they are designated 3.3 V; and on universal boards, they are designated +V (I/O).
2. Pins 12 and 13 are used for a GND key on 5-V-only boards and are connector keys for 3.3-V-only boards.
3. Pin B49 may be designated M66EN for 66-MHz operation.
4. These pins are used for connector keys on 5-V-only boards and are GND for 3.3-V-only boards.

Signal Definitions

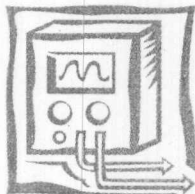
ACK64*	Acknowledge 64-bit Transfer	PERR*	Data parity error
AD00-AD63	Address and data bus	REQx*	Bus request from bus master
C/BEx*	Command and byte enable	RST*	System reset
CLK	Clock	SBO*	Cache snoop back off
DEVSEL*	Device select	SDONE	Cache Snoop Done
FRAME*	Cycle frame	SERR*	System error
GND	Ground	STOP*	Stop transaction
GNTx*	Bus grant	TCK	JTAG Test Signal
INTA*-INTD*	Interrupt request	TDI	JTAG Test Signal
IRDY*	Initiator ready	TDO	JTAG Test Signal
LOCK*	Bus lock	TMS	JTAG Test Signal
PARxx	Parity for ADxx and C/BEx*	TRDY*	Target ready
		TRST*	JTAG Test Signal

*Pin designations that end in * are active low.

Binary Bit Weights

n Bits	States (2 ⁿ)	LSB Weight (1/2 ⁿ)	LSB Weight (ppm)	LSB Weight (% Full Scale)	Bit Weight for 10-V Full Scale	Dynamic Range (dB)
0	1	1	1,000,000	100	10 V	0
1	2	0.5	500,000	50	5 V	6.02
2	4	0.25	250,000	25	2.5 V	12.04
3	8	0.125	125,000	12.5	1.25 V	18.06
4	16	0.0625	62,500	6.25	625 mV	24.08
5	32	0.03125	31,250	3.125	312.5 mV	30.10
6	64	0.015625	15,625	1.5625	156.25 mV	36.12
7	128	0.0078125	7,812.50	0.781250	78.125 mV	42.14
8	256	0.00390625	3,906.25	0.390625	39.0625 mV	48.16
9	512	0.00195313	1,953.123	0.195313	19.5313 mV	54.19
10	1,024	0.000976563	976.563	0.097656	9.76563 mV	60.21
11	2,048	0.000488281	488.281	0.048828	4.88281 mV	66.23
12	4,096	0.000244141	244.141	0.024414	2.44141 mV	72.25
13	8,192	0.00012207	122.070	0.012207	1.22070 mV	78.27
14	16,384	6.10352 x 10 ⁻⁵	61.035	0.006104	610.352 μV	84.29
15	32,768	3.05176 x 10 ⁻⁵	30.518	0.003052	305.176 μV	90.31
16	65,536	1.52588 x 10 ⁻⁵	15.259	0.001526	152.588 μV	96.33
17	131,072	7.62939 x 10 ⁻⁶	7.629	0.000763	76.2939 μV	102.35
18	262,144	3.8147 x 10 ⁻⁶	3.815	0.000381	38.1470 μV	108.37
19	524,288	1.90735 x 10 ⁻⁶	1.907	0.000191	19.0735 μV	114.39
20	1,048,576	9.53674 x 10 ⁻⁷	0.954	0.000095	9.53674 μV	120.41
21	2,097,152	4.76837 x 10 ⁻⁷	0.477	0.000048	4.76837 μV	126.43
22	4,194,304	2.38419 x 10 ⁻⁷	0.238	0.000024	2.38419 μV	132.45
23	8,388,608	1.19209 x 10 ⁻⁷	0.119	0.000012	1.19209 μV	138.47
24	16,777,216	5.96 x 10 ⁻⁸	0.060	0.000006	0.596046 μV	144.49

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